

In the Claims:

1. (Original) An output driver circuit, comprising:
  - a first totem pole driver stage having at least one PMOS pull-up transistor and at least one NMOS pull-down transistor therein that are responsive to a first pull-up signal and a first pull-down signal, respectively;
  - a second totem pole driver stage having at least one NMOS pull-up transistor and at least one PMOS pull-down transistor therein that are responsive to a second pull-up signal and second pull-down signal, respectively; and
  - a first resistive element having a first terminal that is electrically coupled to drain terminals of the at least one PMOS pull-up transistor and the at least one NMOS pull-down transistor and a second terminal that is electrically coupled to source terminals of the at least one NMOS pull-up transistor and the at least one PMOS pull-down transistor.
2. (Original) The driver circuit of Claim 1, wherein the first and second pull-up signals are complementary signals; and wherein the first and second pull-down signals are complementary signals.
3. (Original) The driver circuit of Claim 1, wherein the drain terminals of the at least one PMOS pull-up transistor and the at least one NMOS pull-down transistor are electrically connected together at a first output node.
4. (Original) The driver circuit of Claim 3, wherein the source terminals of the at least one NMOS pull-up transistor and the at least one PMOS pull-down transistor are electrically connected together at a second output node.
5. (Original) The driver circuit of Claim 4, further comprising a second resistive element that is electrically connected between an output terminal of the driver circuit and the second output node.

6. (Original) The driver circuit of Claim 5, wherein a resistance of the second resistive element is less than a resistance of the first resistive element.

7. (Original) The driver circuit of Claim 1, wherein said second totem pole driver stage comprises:

a normally-on PMOS pull-up transistor having a drain terminal electrically connected to a drain terminal of the at least one NMOS pull-up transistor; and  
a normally-on NMOS pull-down transistor having a drain terminal electrically connected to a drain terminal of the at least one PMOS pull-down transistor.

8. (Original) The driver circuit of Claim 1, wherein said at least one PMOS pull-up transistor comprises:

a coarsely tuned array of binary weighted PMOS pull-up transistors in parallel with a finely tuned array of non-binary weighted PMOS pull-up transistors.

9. (Original) The driver circuit of Claim 8, wherein said at least one NMOS pull-down transistor comprises:

a coarsely tuned array of binary weighted NMOS pull-down transistors in parallel with a finely tuned array of non-binary weighted NMOS pull-down transistors.

10. (Original) The driver circuit of Claim 1, wherein said at least one NMOS pull-up transistor comprises:

a coarsely tuned array of binary weighted NMOS pull-up transistors in parallel with a finely tuned array of non-binary weighted NMOS pull-up transistors.

11. (Original) The driver circuit of Claim 10, wherein said at least one PMOS pull-down transistor comprises:

a coarsely tuned array of binary weighted PMOS pull-down transistors in parallel with a finely tuned array of non-binary weighted PMOS pull-down transistors.

12. (Original) The driver circuit of Claim 11, wherein said second totem pole driver stage comprises:

a normally-on PMOS pull-up transistor having a drain terminal electrically connected to a drain terminal of the at least one NMOS pull-up transistor; and

a normally-on NMOS pull-down transistor having a drain terminal electrically connected to a drain terminal of the at least one PMOS pull-down transistor.

13. (Original) The driver circuit of Claim 1, wherein said first resistive element has a resistance in a range from between about 5 ohms and about 15 ohms.

14. (Original) An output driver circuit, comprising:

a first totem pole driver stage having at least one PMOS pull-up transistor and at least one NMOS pull-down transistor therein that are responsive to a first pull-up signal and a first pull-down signal, respectively;

a second totem pole driver stage having at least one NMOS pull-up transistor and at least one PMOS pull-down transistor therein that are responsive to a second pull-up signal and second pull-down signal, respectively; and

a first resistive element having a resistance value in a range from between about 0 ohms and about 20 ohms, said first resistive element having a first terminal that is electrically coupled to drain terminals of the at least one PMOS pull-up transistor and the at least one NMOS pull-down transistor and a second terminal that is electrically coupled to source terminals of the at least one NMOS pull-up transistor and the at least one PMOS pull-down transistor;

wherein said at least one PMOS pull-up transistor comprises:

a coarsely tuned array of binary weighted PMOS pull-up transistors in parallel with a finely tuned array of non-binary weighted PMOS pull-up transistors; and

wherein said at least one NMOS pull-down transistor comprises:

a coarsely tuned array of binary weighted NMOS pull-down transistors in parallel with a finely tuned array of non-binary weighted NMOS pull-down transistors.

15. (Original) The driver circuit of Claim 14, wherein said at least one NMOS pull-up transistor comprises a coarsely tuned array of binary weighted NMOS pull-up transistors in parallel with a finely tuned array of non-binary weighted NMOS pull-up transistors.

Claims 16-19 (Canceled).

20. (Original) An output driver circuit, comprising:

a first totem pole driver stage having at least one PMOS pull-up transistor and at least one NMOS pull-down transistor therein that are responsive to a first pull-up signal and a first pull-down signal, respectively, said at least one PMOS pull-up transistor comprising a coarsely tuned array of binary weighted PMOS pull-up transistors in parallel with a finely tuned array of non-binary weighted PMOS pull-up transistors;

a second totem pole driver stage having at least one NMOS pull-up transistor and at least one PMOS pull-down transistor therein that are responsive to a second pull-up signal and second pull-down signal, respectively, said at least one NMOS pull-up transistor comprising a coarsely tuned array of binary weighted NMOS pull-up transistors in parallel with a finely tuned array of non-binary weighted NMOS pull-up transistors; and

a first resistive element having a resistance value in a range from between about 0 ohms and about 20 ohms, said first resistive element having a first terminal that is electrically coupled to drain terminals of the at least one PMOS pull-up transistor and the at least one NMOS pull-down transistor and a second terminal that is electrically coupled to source terminals of the at least one NMOS pull-up transistor and the at least one PMOS pull-down transistor.

21. (Original) The driver circuit of Claim 20, wherein a pair of PMOS pull-up transistors in the finely tuned array of non-binary weighted PMOS pull-up transistors have widths equal to:  $W+n\beta$  and  $W+(n+1)\beta$ , where  $n$  is a positive integer,  $\beta$  is a positive number,  $W > 4\mu\text{m}$  and  $n\beta < W$ .

22. (Original) The driver circuit of Claim 21, wherein a plurality of PMOS pull-up transistors in the coarsely tuned array of binary weighted PMOS pull-up transistors have widths equal to:  $W$ ,  $2W$  and  $4W$ .

23. (Original) An integrated circuit device, comprising:

a first pull-up path having at least one PMOS pull-up transistor therein that is responsive to a first pull-up signal;

a second pull-up path having at least one NMOS pull-up transistor therein that is responsive to a second pull-up signal; and

a first resistive element having a first terminal that is electrically coupled to a drain terminal of the at least one PMOS pull-up transistor and a second terminal that is electrically coupled to a source terminal of the at least one NMOS pull-up transistor;

wherein said at least one PMOS pull-up transistor comprises:

a coarsely tuned array of binary weighted PMOS pull-up transistors in parallel with a finely tuned array of non-binary weighted PMOS pull-up transistors; and

wherein said at least one NMOS pull-up transistor comprises:

a coarsely tuned array of binary weighted NMOS pull-up transistors in parallel with a finely tuned array of non-binary weighted NMOS pull-up transistors.

24. (Original) An integrated circuit device, comprising:

- a first pull-down path having at least one NMOS pull-down transistor therein that is responsive to a first pull-down signal;
- a second pull-down path having at least one PMOS pull-down transistor therein that is responsive to a second pull-down signal; and
- a first resistive element having a first terminal that is electrically coupled to a drain terminal of the at least one NMOS pull-down transistor and a second terminal that is electrically coupled to a source terminal of the at least one PMOS pull-down transistor;

wherein said at least one NMOS pull-down transistor comprises:

- a coarsely tuned array of binary weighted NMOS pull-down transistors in parallel with a finely tuned array of non-binary weighted NMOS pull-down transistors; and

wherein said at least one PMOS pull-down transistor comprises:

- a coarsely tuned array of binary weighted PMOS pull-down transistors in parallel with a finely tuned array of non-binary weighted PMOS pull-down transistors.

Claims 25-26 (Canceled).

27. (Original) An output driver circuit, comprising:

a first totem pole driver stage having at least one PMOS pull-up transistor and at least one NMOS pull-down transistor therein that are responsive to a first pull-up signal and a first pull-down signal, respectively; and

a second totem pole driver stage having at least one NMOS pull-up transistor and at least one PMOS pull-down transistor therein that are responsive to a second pull-up signal and second pull-down signal, respectively;

wherein said at least one PMOS pull-up transistor comprises:

a coarsely tuned array of binary weighted PMOS pull-up transistors in parallel with a finely tuned array of non-binary weighted PMOS pull-up transistors; and

wherein said at least one NMOS pull-down transistor comprises:

a coarsely tuned array of binary weighted NMOS pull-down transistors in parallel with a finely tuned array of non-binary weighted NMOS pull-down transistors.